

P-Channel JFET



J270 – J271 / SST270 – SST271

FEATURES

- Surface Mount

APPLICATIONS

- P-Channel Amplifier

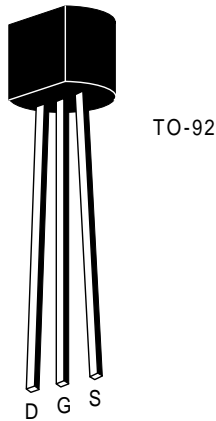
DESCRIPTION

The J270/SST270 Series is an all-purpose amplifier for designs requiring P-channel operation. These devices feature high gain, low noise and tight $V_{GS(OFF)}$ limits for simple circuit design. They are available in low-cost SOT-23 and TO-92 packages and are fully compatible with automatic insertion techniques.

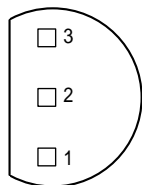
ORDERING INFORMATION

Part	Package	Temperature Range
J270-271	Plastic TO-92	-55°C to +135°C
SST270-271	Plastic SOT-23	-55°C to +135°C

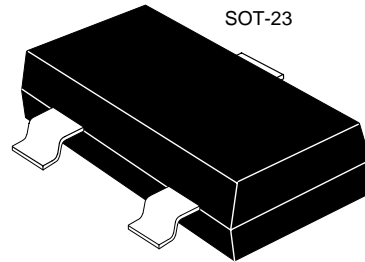
PIN CONFIGURATION



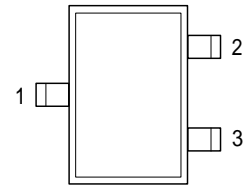
- 1 DRAIN
- 2 GATE
- 3 SOURCE



BOTTOM VIEW



- 1 GATE
- 2 SOURCE
- 3 DRAIN



TOP VIEW

PRODUCT MARKING (SOT-23)

SST270	P20
SST271	P21

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNIT
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	V
Gate Current	I_G	-50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/ $^\circ\text{C}$
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

SYMBOL	PARAMETER	TYP ¹	270		271		UNIT	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
STATIC								
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	45	30		30		V	$I_G = 1\mu\text{A}, V_{DS} = 0\text{V}$
$V_{GS(OFF)}$	Gate-Source Cutoff Voltage		0.5	2.0	1.5	4.5		$V_{DS} = -15\text{V}, I_D = -1\text{nA}$
I_{DSS}	Saturation Drain Current ²		-2	-15	-6	-50	mA	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate Reverse Current	10		200		200	pA	$V_{GS} = 20\text{V}, V_{DS} = 0\text{V}$
		5					nA	$T_A = 125^\circ\text{C}$
I_G	Gate Operating Current	10					pA	$V_{DG} = -15\text{V}, I_D = -1\text{mA}$
$V_{GS(F)}$	Gate-Source Forward Voltage	-0.7					V	$I_G = -1\text{mA}, V_{DS} = 0\text{V}$
DYNAMIC								
g_{fs}	Common-Source Forward Transconductance		6	15	8	18	mS	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{kHz}$
g_{os}	Common-Source Output Conductance			200		500	μS	
C_{iss}	Common-Source Input Capacitance	20					pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
C_{rss}	Common-Source Reverse Transfer Capacitance	4						
e_n	Equivalent Input Noise Voltage	20					$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{kHz}$

NOTES: 1. For design aid only, not subject to production testing.
2. Pulse test; $PW = 300\mu\text{s}$, duty cycle $\leq 3\%$.